AMENDMENTS TO THE CLAIMS:

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Currently Amended) A spread spectrum clock generation circuit comprising: a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock; a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator; a loop-filter for generating a differential signal in accordance with the charge signal; a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the differential signal so that the differential signal changes with an amplitude, which is smaller than that of the differential signal, and with a spread spectrum modulation period which is sufficiently longer than that of the generated clock; and a clock generator for generating the generated clock with a frequency in accordance with the spread spectrum modulation signal, wherein the spread spectrum modulation period of the spread spectrum modulation signal changes so as to have multiple different periods,

wherein the clock generator is a voltage control oscillator,

wherein the spread spectrum modulation circuit comprises an analog modulator for generating a spread spectrum analog voltage signal the period of which changes so as to take multiple different periods, and a voltage addition circuit for adding the spread spectrum analog voltage signal to the differential signal,

~~A spread spectrum clock generation circuit, as set forth in claim 4,~~ wherein the

analog modulator comprises a plurality of different capacitors, a plurality of switches for selecting one of the plurality of different capacitors, a constant current source for supplying a constant current to the selected capacitor or making the constant current flow out of the selected capacitor, a hysteresis comparator for detecting the fact that the voltage of the selected capacitor reaches first and second predetermined voltages and a switch control circuit for switching the selected plurality of switches when the hysteresis comparator detects the fact that the first and second predetermined voltages are reached.

6. (Currently Amended) A spread spectrum clock generation circuit comprising: a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock; a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator; a loop-filter for generating a differential signal in accordance with the charge signal; a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the differential signal so that the differential signal changes with an amplitude, which is smaller than that of the differential signal, and with a spread spectrum modulation period which is sufficiently longer than that of the generated clock; and a clock generator for generating the generated clock with a frequency in accordance with the spread spectrum modulation signal, wherein the spread spectrum modulation period of the spread spectrum modulation signal changes so as to have multiple different periods,

wherein the clock generator is a voltage control oscillator,

~~A spread spectrum clock generation circuit, as set forth in claim 3,~~ wherein the spread spectrum modulation circuit comprises a digital control circuit for generating an output code the period of which changes so as to take multiple different periods,

a voltage digital-to-analog conversion circuit for generating a spread spectrum voltage signal in accordance with the output code, and a voltage addition circuit for adding the spread spectrum voltage signal to the differential signal.

7. (Currently Amended) A spread spectrum clock generation circuit comprising: a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock; a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator; a loop-filter for generating a differential signal in accordance with the charge signal; a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the differential signal so that the differential signal changes with an amplitude, which is smaller than that of the differential signal, and with a spread spectrum modulation period which is sufficiently longer than that of the generated clock; and a clock generator for generating the generated clock with a frequency in accordance with the spread spectrum modulation signal, wherein the spread spectrum modulation period of the spread spectrum modulation signal changes so as to have multiple different periods, ~~A spread spectrum clock generation circuit, as set forth in claim 1,~~ wherein a voltage-current conversion circuit for converting the differential signal, which is a voltage signal, into a differential current signal is further comprised, the clock generator is a current control oscillator, and the spread spectrum modulation circuit comprises a digital control circuit for generating an output code the period of which changes so as to have multiple different periods and a current variable circuit provided between the voltage-current conversion circuit and the current control oscillator and which generates a spread spectrum current modulation signal by modulating the differential current signal in accordance with the output code.

8. (Original) A spread spectrum clock generation circuit, as set forth in claim 7, wherein the current variable circuit comprises a circuit for generating the differential current signal in a predetermined ratio and a current digital-to-analog conversion circuit for converting the output code into a spread spectrum current signal, which is an analog signal, and adding the analog signal to the differential current signal.

9. (Original) A spread spectrum clock generation circuit, as set forth in claim 6, wherein the digital control circuit comprises a plurality of dividers with a different dividing ratio with which a clock is divided, a switch controller for selecting the output of the plurality of dividers in order, an up/down counter for counting the selected dividing clock, and a counter for switching between the up operation and the down operation of the up/down counter for each predetermined count number by counting the dividing clock.

10. (Original) A spread spectrum clock generation circuit, as set forth in claim 7, wherein the digital control circuit is a computer system controlled by programs.

11. (Canceled)

12. (Original) A spread spectrum clock generation circuit comprising: a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock; a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator; a loop-filter for generating a differential signal in accordance with the charge signal; a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the differential signal so that the differential signal changes with an amplitude, which is smaller than that of the differential signal, and with a spread spectrum modulation period which is

sufficiently longer than that of the generated clock; and a clock generator for generating a generated clock with a frequency in accordance with the spread spectrum modulation signal, wherein the spread spectrum modulation signal has a waveform in which a local maximum and/or a local minimum, of a signal value, change.

13. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein the spread spectrum modulation signal has a triangular waveform of which the amplitude changes.

14. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein the spread spectrum modulation signal has a triangular waveform of which the mean level changes.

15. (Original) A spread spectrum clock generation circuit, as set forth in claim 13, wherein the spread spectrum modulation signal further changes the spread spectrum modulation period.

16. (Original) A spread spectrum clock generation circuit, as set forth in claim 14, wherein the spread spectrum modulation signal further changes the spread spectrum modulation period.

17. (Original) A spread spectrum clock generation circuit, as set forth in claim 13, wherein the spread spectrum modulation signal changes the amplitude for each period in order.

18. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein the clock generator is a voltage control oscillator.

19. (Original) A spread spectrum clock generation circuit, as set forth in claim 18, wherein the spread spectrum modulation circuit comprises an analog modulator for generating a spread spectrum analog voltage signal the local maximum and

minimum of the amplitude of which changes so as to take multiple different values in order, and a voltage addition circuit for adding the spread spectrum analog voltage signal to the differential signal.

20. (Original) A spread spectrum clock generation circuit, as set forth in claim 18, wherein the analog modulator comprises a constant current source for switching between a state in which the capacitor is charged with a constant current and a state in which a constant current is discharged from the capacitor, and a switch control circuit for changing the switching cycle of the constant current source.

21. (Original) A spread spectrum clock generation circuit, as set forth in claim 18, wherein the spread spectrum modulation circuit comprises: a digital control circuit for generating an output code which changes to continuously repeat an increase and a decrease; a voltage digital-to-analog conversion circuit for generating a spread spectrum voltage signal in accordance with the output code; and a voltage addition circuit for adding the spread spectrum voltage signal to the differential signal.

22. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein a voltage-current conversion circuit for converting the differential signal, which is a voltage signal, into a differential current signal is further comprised, the clock generator is a current control oscillator, and the spread spectrum modulation circuit comprises: a digital control circuit for generating an output code which changes to continuously repeat an increase and a decrease; and a current variable circuit which is provided between the voltage-current conversion circuit and the current control oscillator and which generates a spread spectrum current modulation signal by modulating the differential current signal in accordance with the output code.

23. (Original) A spread spectrum clock generation circuit, as set forth in claim 22, wherein the current variable circuit comprises a current digital-to-analog conversion circuit for converting the output code into a spread spectrum current signal, which is an analog signal, and adding the converted signal to the differential current signal.

24. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein a voltage-current conversion circuit for converting the differential signal, which is a voltage signal, into a differential current signal is further comprised, the clock generator is a current control oscillator, the spread spectrum modulation circuit comprises: a digital control circuit for generating a spectrum modulation code the value of which changes to continuously repeat an increase and a decrease and a level change code the value of which changes so as to take multiple different values; a first current variable circuit which is provided between the voltage-current conversion circuit and the current control oscillator and which modulates a current signal in a predetermined ratio of the differential current signal in accordance with the spectrum modulation code; and a second current variable circuit for amplifying the output of the first current variable circuit in accordance with the level change code, wherein the output of the second current variable circuit is added to the differential current signal.

25. (Original) A spread spectrum clock generation circuit, as set forth in claim 12, wherein a voltage-current conversion circuit for converting the differential signal, which is a voltage signal, into a differential current signal is further comprised, the clock generator is a current control oscillator, the spread spectrum modulation circuit comprises a digital control circuit for generating a spectrum modulation code the value of which changes to continuously repeat an increase and a decrease and a

level change code the value of which changes so as to take multiple different values; a first current variable circuit which is provided between the voltage-current conversion circuit and the current control oscillator and which amplifies a current signal in a predetermined ratio of the differential current signal in accordance with the level change code; and a second current variable circuit for modulating the output of the first current variable circuit in accordance with the spectrum modulation code, wherein the output of the second current variable circuit is added to the differential current signal.

26. (Original) A spread spectrum clock generation circuit, as set forth in claim 22, wherein the digital control circuit comprises a plurality of dividers with a different dividing ratio with which a clock is divided, a switch controller for selecting the output of the plurality of dividers in order, an up/down counter for counting the selected dividing clock, and a counter for switching between the up operation and down operation of the up/down counter for each determined count number by counting the dividing clock.

27. (Original) A spread spectrum clock generation circuit, as set forth claim 22, wherein the digital control circuit is a computer system controlled by programs.

28. (Withdrawn) A spread spectrum clock generation circuit comprising a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock, a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator, a loop-filter for generating a differential voltage signal in accordance with the charge signal, a voltage-current conversion circuit for converting the differential voltage signal into a differential current signal, and a clock generator for generating a generated clock with a frequency in accordance with the

differential current signal, wherein a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the differential current signal and an amplifier circuit for amplifying the spread spectrum modulation signal are comprised and the amplified spread spectrum modulation signal is added to the differential current signal and applied to the clock generator.

29. (Withdrawn) A spread spectrum clock generation circuit comprising a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock, a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator, a loop-filter for generating a differential voltage signal in accordance with the charge signal, a voltage-current conversion circuit for converting the differential voltage signal into a differential current signal, and a clock generator for generating a generated clock with a frequency in accordance with the differential current signal, wherein an amplifier circuit for amplifying the differential current signal and a spread spectrum modulation circuit for generating a spread spectrum modulation signal by modulating the amplified differential current signal are comprised and the spread spectrum modulation signal is added to the differential current signal and applied to the clock generator.

30. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 28, wherein the spread spectrum modulation circuit comprises a digital control circuit for generating an output code which changes continuously between the maximum value and the minimum value and a current digital-to-analog conversion circuit for changing an input current signal in accordance with the output code.

31. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 28, wherein the amplifier circuit comprises a digital control circuit, for

generating a constant output code, and a current digital-to-analog conversion circuit, for changing an input current signal to a current in accordance with the output code.

32. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 30, wherein the current digital-to-analog conversion circuit is a circuit comprising a transistor train each of which generates a current in accordance with the input current with a weighting ratio corresponding to the output code and outputs an output current to which the current output from the transistor train is added, and the output of the current of each transistor of the transistor train is changed to a current in accordance with the output code by the control in accordance with the output code.

33. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 30, wherein the digital control circuit comprises a plurality of dividers with a different dividing ratio with which a clock is divided, a switch controller for selecting the output of the plurality of dividers in order, an up/down counter for counting the selected dividing clock, and a counter for switching between the up operation and the down operation of the up/down counter for each predetermined count number by counting the dividing clock.

34. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 30, wherein the digital control circuit is a computer system controlled by programs.

35. (Withdrawn) A spread spectrum clock generation circuit comprising a frequency phase comparator for detecting a difference in phase between a reference clock and a generated clock, a charge pump for generating a charge/discharge signal in accordance with the difference in phase detected by the frequency phase comparator, a loop-filter having a resistor and a capacitor

connected in series between the output of the charge pump and a predetermined potential and which generates a differential voltage signal in accordance with the charge signal, a clock generator for generating a generated clock with a frequency in accordance with the differential voltage signal, and a current injection circuit connected to the connection node of the resistor and the capacitor of the loop-filter and which charges and discharges the capacitor so that the voltage of the capacitor changes with an amplitude smaller than the voltage of the capacitor and in a spread spectrum period longer than the period of generated clock.

36. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 35, wherein the current injection circuit comprises a push-pull type current source for generating charging and discharging currents for the capacitor and a current source control circuit for controlling the push-pull type current source.

37. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 36, wherein the clock generator comprises a V - I conversion circuit for converting the differential voltage signal into a differential current signal and a current control oscillation circuit for generating a generated clock with a frequency in accordance with the differential current signal, and the push-pull type current source charges or discharges the capacitor with an amount of charging or discharging current in accordance with the differential current signal output from the V - I conversion circuit.

38. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 37, wherein a low-pass filter for generating a filtering differential current signal by filtering the high-frequency component from the differential current signal output from the V - I conversion circuit is comprised, and the push-pull type current source changes or discharges the capacitor with an amount of charging or discharging

current in accordance with the filtering differential current signal.

39. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 36, wherein a low-pass filter for generating a filtering differential voltage signal by filtering the high-frequency component from the differential voltage signal and a filtering V - I conversion circuit for converting the filtering differential voltage signal into a filtering differential current signal are comprised, and the push-pull type current source charges or discharges the capacitor with an amount of charging or discharging current in accordance with the filtering differential current signal.

40. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 35, wherein the current injection circuit comprises a digital control circuit for generating an output code which changes in a period in accordance with the spread spectrum modulation period, and a push-pull type current digital-to-analog conversion (IDAC) circuit for generating charging and discharging currents in accordance with the output code.

41. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 40, wherein the clock generator comprises a V - I conversion circuit for converting the differential voltage signal into a differential current signal and a current control oscillation circuit for generating a generated clock with a frequency in accordance with the differential current signal, and the push-pull type current digital-to-analog conversion circuit charges or discharges the capacitor with an amount of charging or discharging current in accordance with the differential current signal output from the V - I conversion circuit.

42. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 41, wherein a low-pass filter for generating a filtering differential signal by filtering the high-frequency component from the differential current signal output

from the V - I conversion circuit is comprised, and the push-pull type current digital-to-analog conversion circuit charges or discharges the capacitor with an amount of charging or discharging current in accordance with the filtering differential current signal.

43. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 40, wherein a low-pass filter for generating a filtering differential voltage signal by filtering the high-frequency component from the differential voltage signal and a filtering V - I conversion circuit for converting the filtering differential voltage signal into a filtering differential current signal are comprised, and the push-pull type current digital-to-analog conversion circuit charges or discharges the capacitor with an amount of charging or discharging current in accordance with the filtering differential current signal.

44. (Withdrawn) A spread spectrum clock generation circuit, as set forth in claim 36, wherein the current injection circuit comprises a reference current source for setting the amount of charging or discharging current.

45. (Withdrawn) A jitter generation circuit for inputting a reference input signal the voltage level of which changes in a constant period and outputting the reference input signal after adding a jitter thereto, the jitter generation circuit comprising a circuit for changing an output to a first level or a second level in accordance with the reference input signal, wherein the circuit is formed so as to be capable of changing the threshold voltage and an output signal with a jitter added is output by changing the threshold voltage.

46. (Withdrawn) A jitter generation circuit, as set forth in claim 45, wherein a hysteresis inverter circuit having the hysteresis characteristic, an inverter circuit not having the hysteresis characteristic, and a switch circuit provided between an output

terminal for outputting the output signal and the hysteresis inverter circuit and between the output terminal and the inverter circuit respectively are comprised and the switch circuit switches the connections so that either the hysteresis inverter circuit or the inverter circuit is connected to the output terminal.

47. (Withdrawn) A jitter generation circuit, as set forth in claim 45, wherein a hysteresis inverter circuit consisting of a plurality of transistors and a switch for cutting off the transistors, which are provided in order to confer hysteresis on the hysteresis inverter circuit, from the hysteresis inverter circuit are comprised.

48. (Withdrawn) A jitter generation circuit, as set forth in claim 45, wherein a plurality of gate circuits with different threshold voltages are connected in parallel and any one of the gate circuits is selectively connected to the output terminal by a switch circuit provided between an output terminal for outputting the output signal and each gate circuit.

49. (Withdrawn) A semiconductor device comprising the jitter generation circuit set forth in claim 45 and an internal circuit which operates based on an output signal output from the jitter generation circuit.

50. (Withdrawn) A semiconductor device, as set forth in claim 49, wherein a clock generation circuit for generating a clock signal as the reference input signal and a circuit provided between the clock generation circuit and the jitter generation circuit and which changes the shape of the clock signal changing in a rectangular wave form to a sinusoidal wave form.

51. (Withdrawn) A semiconductor device, as set forth in claim 49, wherein a clock generation circuit for generating a clock signal as the reference input signal and a selection signal generation circuit for generating a selection signal based on the reference input signal generated in the clock generation circuit are comprised

and the threshold voltages are switched by the selection signal.

52. (Withdrawn) A semiconductor device comprising the jitter generation circuit set forth in claim 45, a first internal circuit to which a clock signal to be an input signal to the jitter generation circuit is supplied, and a second internal circuit the operation timing of which is less strict than that of the first internal circuit and to which a clock signal with a jitter added in the jitter generation circuit is supplied.

53. (Withdrawn) A semiconductor device comprising a jitter generation circuit for inputting a clock signal and outputting the clock signal after adding a jitter thereto, a first internal circuit to which a lock signal to be an input signal to the jitter generation circuit is supplied, and a second internal circuit the operation timing of which is less strict than that of the first internal circuit and to which a clock signal, with a jitter added in the jitter generation circuit, is supplied.

54. (Withdrawn) A semiconductor device, as set forth in claim 52, wherein a dividing circuit is comprised for generating and inputting to the jitter generation circuit a second clock signal, the frequency of which is lower than that of a first clock signal, by dividing the first clock signal which is used to operate the first internal circuit.

55. (Withdrawn) A semiconductor device, as set forth in claim 52, wherein a plurality of the jitter generation circuits are comprised and the amount of jitter to be added to a clock signal is made differ from each other in each jitter generation circuit.

56. (Withdrawn) A semiconductor device, as set forth in claim 52, wherein the jitter generation circuit has a function for adjusting the amount of jitter to be added to a clock signal in accordance with the condition of operation of the internal circuit.

57. (Withdrawn) A semiconductor device, as set forth in claim 56, wherein the amount of jitter in the jitter generation circuit is adjusted in accordance with the power supply voltage to the internal circuit.

58. (Withdrawn) A semiconductor device, as set forth in claim 56, wherein the amount of jitter in the generation circuit is adjusted in accordance with the operation speed of the internal circuit.

59. (Withdrawn) A semiconductor device, as set forth in claim 55, wherein a first jitter generation circuit for adding a jitter to a clock signal and a second jitter generation circuit for further adding a jitter to the clock signal with the jitter added are comprised.

60. (Withdrawn) A semiconductor device, as set forth in claim 55, wherein a first jitter generation circuit and a second jitter generation circuit to which a clock signal the frequency of which is lower than the first jitter generation circuit is input are comprised and the second jitter generation circuit adds a jitter larger than that of the first jitter generation circuit.